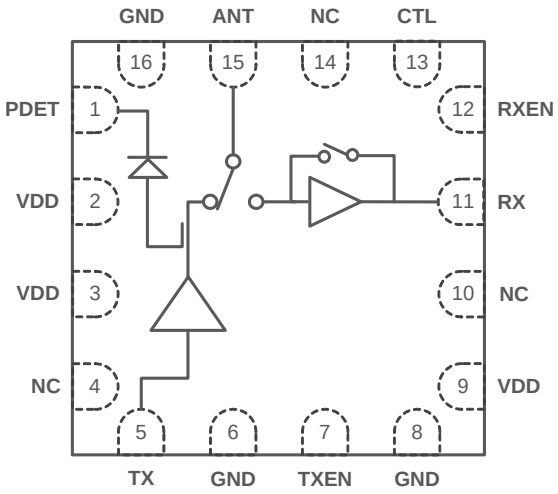
CMOS 5GHz WLAN 802.11ac RFeIC with PA, LNA and SPDT



Description

RFX8053 is a highly integrated, single-chip, single-die RFeIC (RF Front-end Integrated Circuit) which incorporates key RF functionality needed for IEEE 802.11a/n/ac WLAN system operating in the 5.15-5.825GHz range. The RFX8053 architecture integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in a CMOS single-chip device.

RFX8053 has simple and low-voltage CMOS control logic, and requires minimal external components. A directional coupler based power detect circuit is also integrated for accurate monitoring of output power from the PA.

RFX8053 is assembled in an ultra-compact low-profile 2.5x2.5x0.45 mm(Max) 16-lead QFN package. With support to direct battery operation, the RFX8053 is ideal RF front-end solution for implementing 5GHz WLAN in smartphones and other mobile platforms.

Applications

- 802.11a/n/ac
- Smartphones
- Tablets/MIDs
- Gaming
- Notebook/Netbook/Ultrabooks
- Mobile/Portable Devices
- Consumer Electronics
- Other 5GHz ISM Platforms

FEATURES

- 5GHz WLAN Single Chip, Single-Die RF Front-End IC
- High Transmit Signal Linearity Meeting Standards for 802.11ac OFDM /MCS9 Modulation
- Separate TX and RX Transceiver Port and Single Antenna Port
- 5GHz Power Amplifier with Low-Pass Harmonic Filter
- Low Noise Amplifier with Bypass Mode
- Transmit/Receive Switch Circuitry
- Integrated Power Detector for Transmit Power Monitor and Control
- Low Voltage (1.2V) CMOS Control Logic
- ESD Protection Circuitry on All Pins
- DC Decoupled RF Ports
- Internal RF Decoupling on All VDD Bias Pins
- Low Noise Figure for the Receive Chain
- High Power Capability for Received Signals in Bypass Mode
- Very Low DC Power Consumption
- Full On-chip Matching Circuitry
- Minimal External Components Required
- 50-Ohm Input / Output Matching
- Market Proven CMOS Technology
- 2.5mm x 2.5mm x 0.45mm(Max) Small Outline 16L QFN Package with Exposed Ground Pad

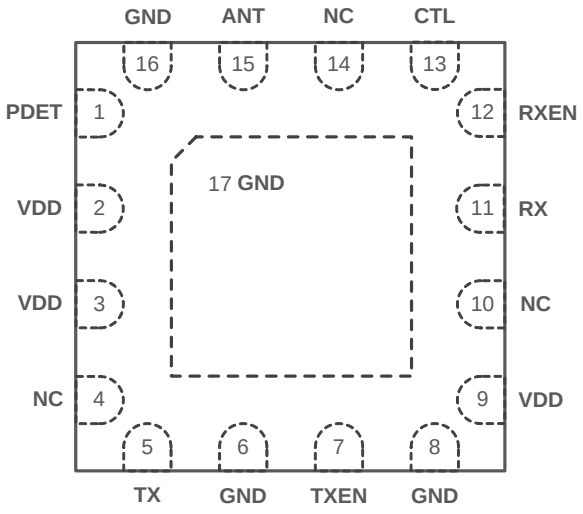
Skyworks Solutions, Inc. • Phone [781] 376-3000 • Fax [781] 376-3100 • sales@skyworksinc.com • www.skyworksinc.com

Rev 2.2
Mar '16

PIN ASSIGNMENTS:

Pin Number	Pin Name	Description
1	PDET	Analog Voltage Proportional to the PA Power Output
4, 10, 14	NC	Not Connected Internally
5	TX	RF Input Port from the Transceiver – DC Shorted to GND
6, 8, 16, 17	GND	Ground – Must Be Connected to GND in the Application Circuit
7	TXEN	CMOS Input to Control TX Enable
2, 3, 9	VDD	DC Supply Voltage
11	RX	RF Output Port from LNA or Bypass – DC Shorted to GND
12	RXEN	CMOS Input to Control RX Enable
13	CTL	CMOS Input for Additional TX Control
15	ANT	Antenna Port RF Signal from the PA or RF Signal Applied to the LNA or Bypass – DC Shorted to GND

PIN-OUT DIAGRAM:



(Top “See-Through” View)

ABSOLUTE MAXIMUM RATINGS:

Parameters	Units	Min	Max	Conditions
DC VDD Voltage Supply	V	0	5.5	All VDD Pins
DC Control Pin Voltage	V	0	3.6	All Control Pins
DC VDD Current Consumption	mA		400	Through VDD Pins when TX is "ON"
TX RF Input Power	dBm		+7	
ANT RF Input Power	dBm		+10	Bypass Mode
Junction Temperature	^oC		150	
Storage Ambient Temperature	^oC	-40	+150	Appropriate care required according to JEDEC Standards
Operating Temperature	^oC	-40	+85	Case Temperature
ESD (HBM)	V	1000		

Note: Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended.

All Maximum RF Input Power Ratings assume 50-Ohm terminal impedance.

NOMINAL OPERATING CONDITIONS:

Parameters	Units	Min	Typ	Max	Conditions
DC VDD Voltage Supply *(Note 1)*	V	3.0	3.6	4.8	All VDD Pins
Control Voltage "High" *(Note 2)*	V	1.2		*	* 3.6V or VDD Whichever is Lower
Control Voltage "Low"	V	0		0.3	
DC Control Pin Current Consumption	µA		1		
DC Shutdown Current	µA		3	10	
PA Turn On/Off Time	µsec			0.4	
θ_{jc} *(Note 3)*	$^oC/W$		28		
θ_{ja}	$^oC/W$		44		
Antenna Switch Speed	µsec			0.4	

Note 1: For normal operation of the RFX8053, VDD must be continuously applied to all VDD supply pins.
Note 2: If control voltage can exceed 1.8V, a 1KΩ – 10KΩ series resistor is recommended for the application circuit on each control line.
Note 3: Thermal measurements were performed on an RFaxis test EVB under typical use conditions. Please contact RFaxis for details regarding the test conditions and the configuration of the thermal vias on the EVB. Refer to "PCB Land Pattern" for recommended thermal vias.

TRANSMIT PATH CHARACTERISTICS (VDD=3.6V; T=+25 °C)

Parameters	Units	Min	Typ	Max	Conditions
Operating Frequency Band	GHz	5.15		5.825	
Linear Output Power for 802.11ac	dBm	+16.5	+17		EVM -35dB, 802.11ac, MCS9, VHT80
Linear Output Power for 802.11n	dBm		+18		EVM -32dB, 802.11n, MCS7, HT40
Linear Output Power for 802.11a	dBm		+19		EVM 3.5%, 802.11a, QAM64, 54 Mbps
Linear Output Power for 802.11a 6Mbps	dBm		+21		For 802.11a 6Mbps Mask Compliance
Small-Signal Power Gain	dB		28		Between TX and ANT pins
Gain Flatness	dB		+/-1		Between 5.15 – 5.85 GHz
TX Quiescent Current	mA		210		
TX Linear Current	mA		270		P_{OUT} = +18dBm
Out-of-Band Rejection	dBc	-10	-15		At 3.9 – 7.2 GHz, relative to in-band gain
Power Detector Voltage Output	mV	300		1600	P_{OUT} = +5 to +20dBm, 10kΩ Load
Second Harmonic	dBc		-35		P_{OUT}=+19dBm, CW
Third Harmonic	dBc		-50		P_{OUT}=+19dBm, CW
Input Return Loss	dB		-10		At TX Port
Output Return Loss	dB		-10		At ANT Port
Load VSWR for Stability (CW, Fix Pin for Pout=+21dBm with 50Ω load)	N/A	4:1	6:1		All non-harmonically related spurs less than -43dBm/MHz
Load VSWR for Ruggedness (CW, Fix Pin for Pout=+21dBm with 50 Ohm Load)	N/A	8:1	10:1		No Damage

RECEIVE PATH CHARACTERISTICS (VDD=3.6V; T=+25 °C)

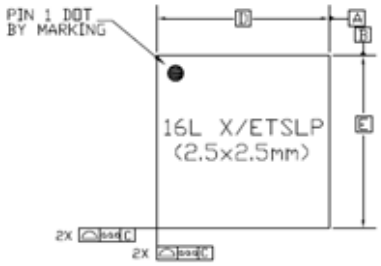
Parameters	Units	Min	Typ	Max	Conditions
Operating Frequency Band	GHz	5.15		5.85	All RF Pins are Loaded by 50-Ohm
Gain	dB	10	12		High Gain Mode, Between ANT and RX pins; RXEN= High, CTL=Low
Noise Figure	dB		3.1		High Gain Mode, At ANT Pin
Insertion Loss for LNA Bypass Mode	dB		5		Between ANT and RX Pins; RXEN=Low, CTL=Low
Input Return Loss	dB		-6		At ANT Port, High Gain Mode
			-10		Bypass Mode
Output Return Loss	dB		-6		At RX Port, High Gain Mode
			-8		Bypass Mode
RF Port Impedance	Ohm		50		
DC Quiescent Current	mA		16		No RF Applied, Through VDD, High Gain Mode
			0.003		No RF Applied, Through VDD, Bypass Mode
IIP3	dBm		+6		At ANT Pin, High Gain Mode
			+20		At ANT Pin, Bypass Mode

CONTROL LOGIC TRUTH TABLE

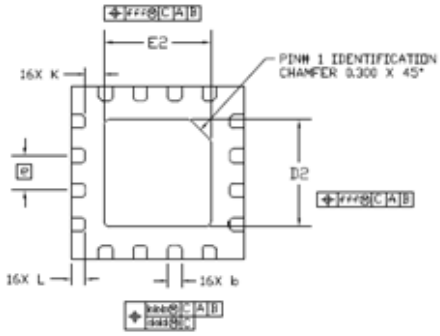
TXEN	CTL	RXEN	Mode Of Operation
0	0	0	Receive Bypass Mode
0	0	1	Receive Mode, High-Gain
1	X	0	Transmit Mode
All Others			Not Specified

Note: "1" denotes high voltage state (> 1.2V)
"0" denotes low voltage state (<0.3V) at Control Pins
"X" denotes don't care, high or low state
1KΩ – 10KΩ series resistor may be required for each control line

PACKAGE DIMENSIONS (All Dimensions in mm):



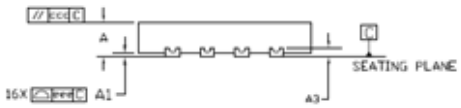
TOP VIEW



BOTTOM VIEW

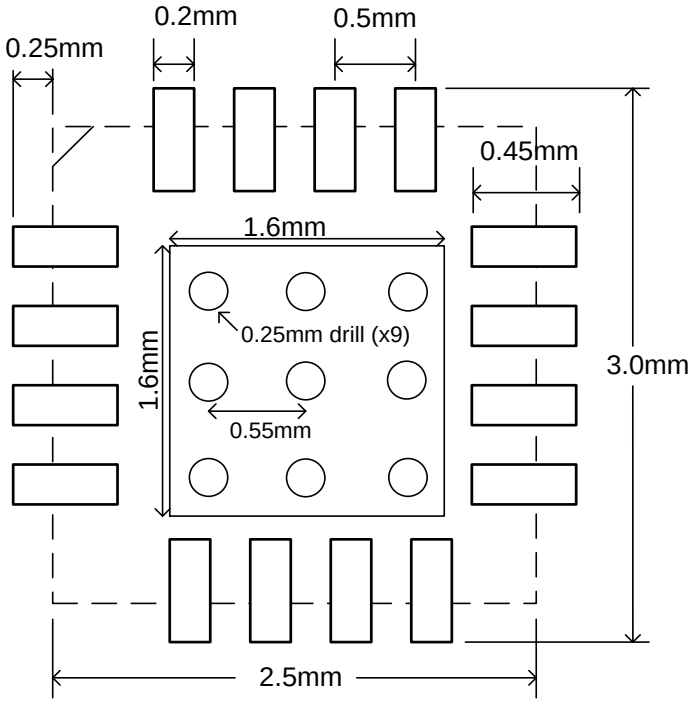
Dimensional Ref.			
REF.	Min.	Nom	Max.
A	—	—	—
	—	—	—
	—	—	0.450
A1	0.000	—	0.050
A3	0.127 BSC		
D	2.500 BSC		
E	2.500 BSC		
D2	1.500	1.550	1.600
E2	1.500	1.550	1.600
b	0.150	0.200	0.250
e	0.500 BSC		
K	0.200	—	—
L	0.175	0.225	0.275
	Dimensional Tol.		
aaa	0.050		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

Notes
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
2. Dimension "A" exclude burr.



SIDE VIEW

PCB LAND PATTERN
(With Recommended Thermal Vias)



PACKAGE MARKING